MEMORY DEVICE FOR COMPENSATING FOR A CLOCK SKEW CAUSING A CENTERING ERROR AND A METHOD OF COMPENSATING FOR THE CLOCK SKEW

Abstract of the Disclosure

The present invention comprises a memory device for compensating for a clock skew that generates a centering error, and a method of compensating for the clock skew. To compensate for a clock skew that causes a centering error between an external clock signal and an output data signal, the memory device includes a phase detector (PD) and an up-down counter. The PD detects a phase difference between the output data signal and the external clock signal and generates an up signal or a down signal depending on the detected phase difference. The up-down counter is enabled by a calibration signal that directs a compensation of the skew and generates an offset code in response to the up signal or the down signal. The offset code is fed back to a delay locked loop (DLL) circuit and aligns the middle points of the output data signal with the edges of the external clock signal.